SPECIAL PURPOSE HARDWARE FOR IMAGE PROCESSING

CSCI 8810 –IMAGE PROCESSING AND COMPUTER GRAPHICS

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TOPICS TO BE COVERED:

1. Why special purpose hardware for Image Processing?

2. Special hardwares in use ?

3. Reconfigurable Hardware
- Why?
- Kinds of Reconfiguration involved
- Advantages.
- Disadvantages.

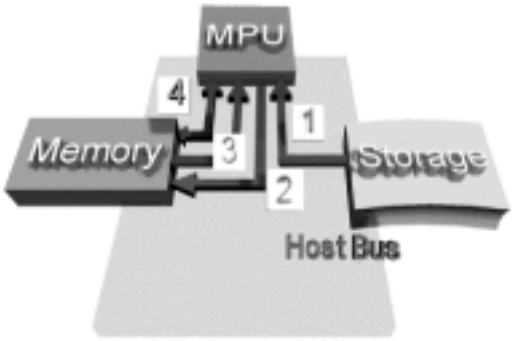
4. Papers in this area
- Hardware Accelerator for Image processing
- Piperench

Why Special purpose hardware for image processing?

- Faster processing
- Less power usage
- Kind of processing

<u>Faster processing</u>

a. General purpose processors



1. Instruction fetch
2. Instruction decode/operands list
3. Operand fetch
4. Execute and write back

    - Average 4 clock cycles

b. Dedicated signal and image processors are faster.

Definition: Processor specially for signal/image processing. **Programmable**

- Absence of instruction fetch/decode => faster
- Most processors have in-built memory => faster operand fetching
- Flip side: some of the generality is lost => problem?

c. ASIC

Definition: Integrated Circuit specially for an application and specific to that. **Non programmable**

- Absence of instruction fetch/decode => faster
- Can have any type of in-built hardware that can potentially improve performance
- Flip side: no generality at all => problem?

Problems:
Image Standards may change.
Processing algorithm may change
Size of the image under consideration may change

What if:
ASIC has to be re-designed.
Redesign time ~ 8 months

SO.
- need for hardware that is not too specific (high cost of maintenance) or not too general (slow)
- need for hardware that is not specific to an application and still behaves like ASIC
- is “Reconfigurable hardware” the answer ?

Low power utilization

Cardinal rule:

Power ∝ number of clock cycles

Lesser the number of clock cycles to an operation, lesser will be the power utilized for that. IP needs significant processing power.

- ⇨ GPP is not a good choice
- ⇨ ASIC is the best choice
- ⇨ What about “Reconfigurable hardware”?

Kind of processing

Image processing is inherently parallel.

Do you agree?

GPP is not suitable for parallel processing.
DSP/DIP- can be programmed to behave parallel
Parallel computers- obviously a good choice

Yet another reason for having special purpose hardware for Image processing

Can a "Reconfigurable hardware" help in this too?

Special hardware in use:

1. Digital Signal/Image processors
2. ASIC
3. Parallel computers: Multi-processor environment
4. Reconfigurable hardware

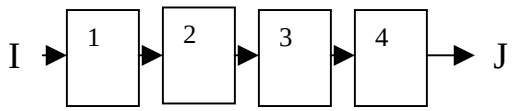
OK. What is Reconfigurable hardware?

Enough suspense……..

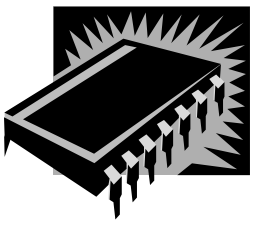
Reconfigurable hardware:
Hardware whose architecture is modified by software to suit application

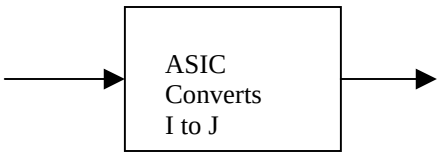
- Large number of Functional Units (FU) with programmable interconnections
- Functionality of the hardware is determined by how interconnections between FUs are configured and how FUs are configured
- Changing the *configuration*, the hardware can be made to perform a completely different function

Example:

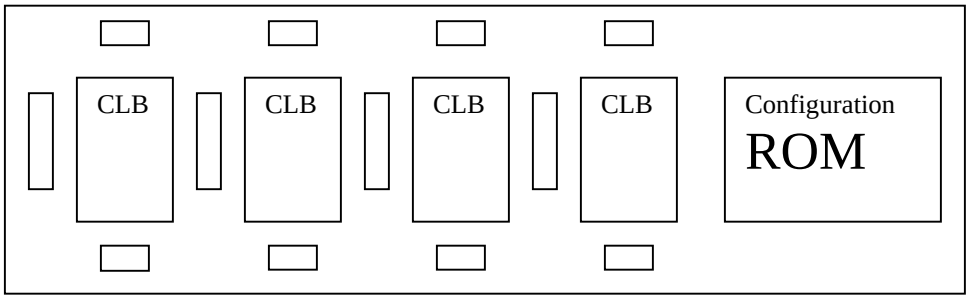


1. Smooth image
2. Robert's mask
3. Converting to BW
4. Component Labelling

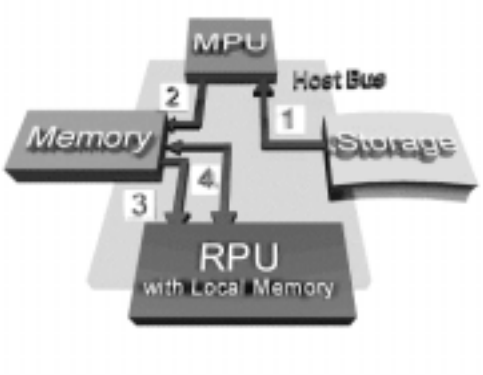




Reconfigurable hardware:

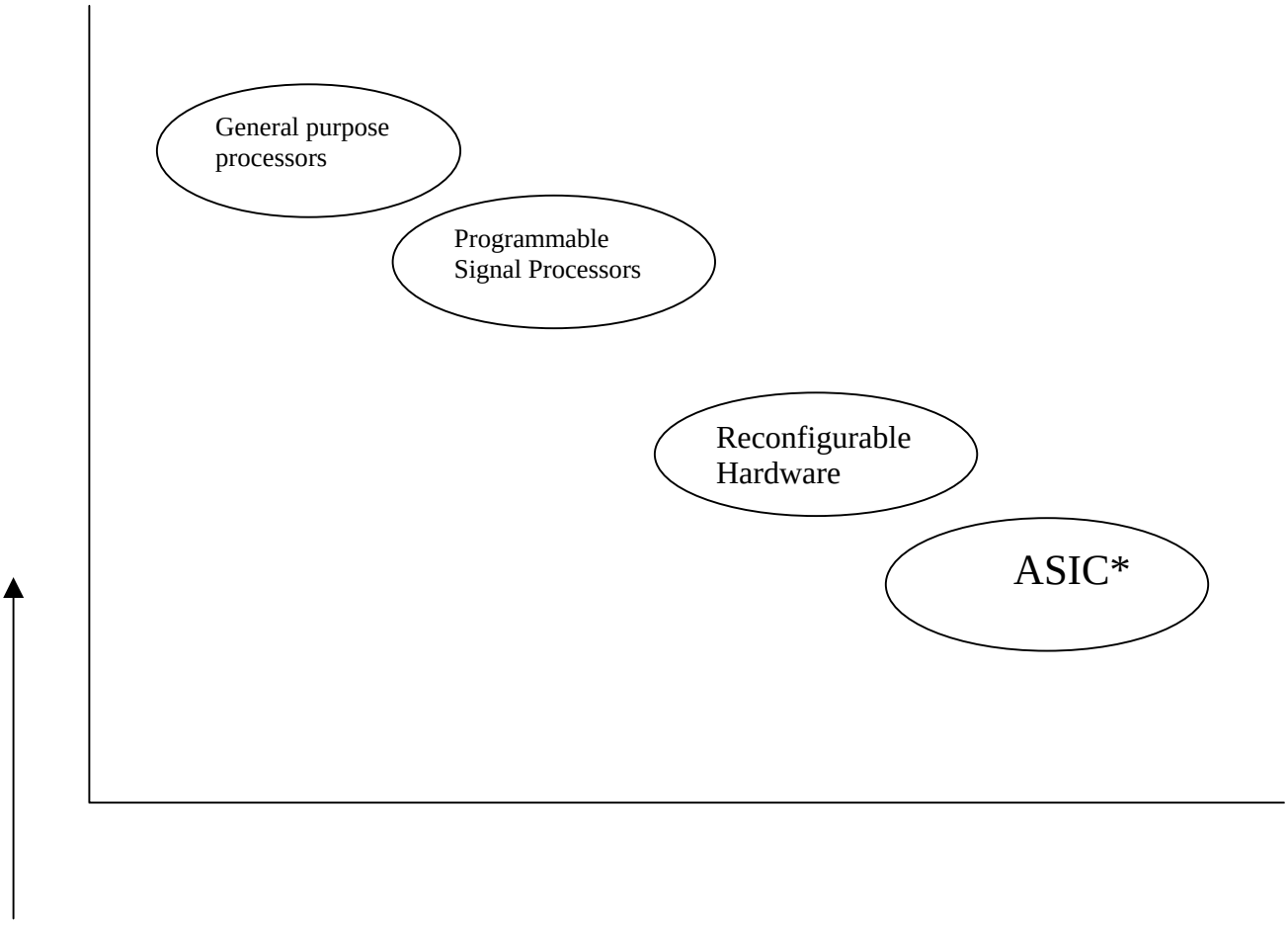


- *Configuration* could be one-time during power-on (Static reconfiguration) OR could be during every clock cycle (Dynamic reconfiguration)
- Uses FPGA- Field Programmable Gate Arrays
- Programming interconnection thru Programmable Switches
- Programmable IOs to interact with outside world
- Configuration ROM to store the configuration: Memory inside each block is Volatile



IS THAT ALL?

Digital Signal / Image processing hardware spectrum



*Application Specific Integrated Circuits

Improving existing architecture: Simple Mesh

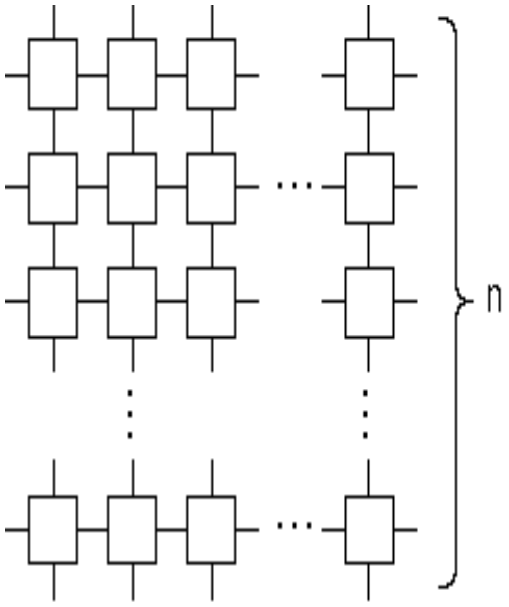


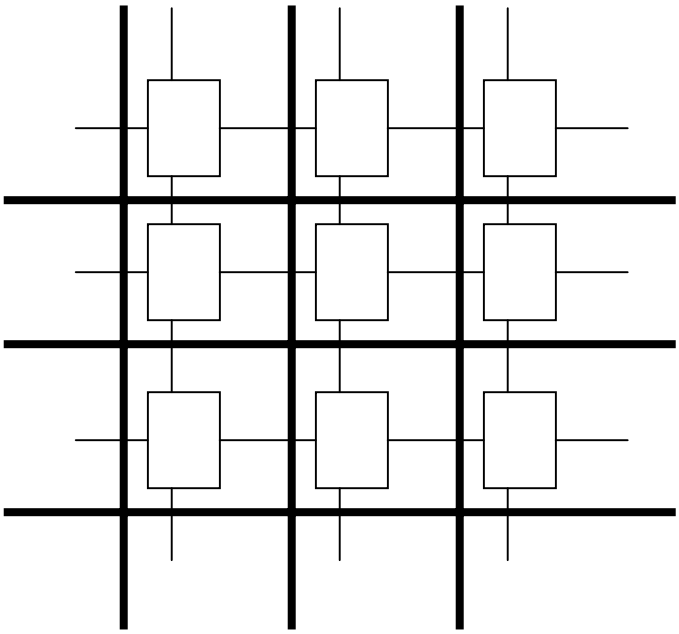
Figure 2

Finding MAX of A, B, C

1. Store A in (1,1)
2. Store B in (1,2)
3. Store C in (1,3)
4. (1,2) gets A from (1,1) and Compares with B. Sends maximum value MAX to (1,3)
5. (1,3) gets MAX from (1,2), compares with C. Returns max value

Time complexity is $O(n^2)$.

Mesh with Bus:



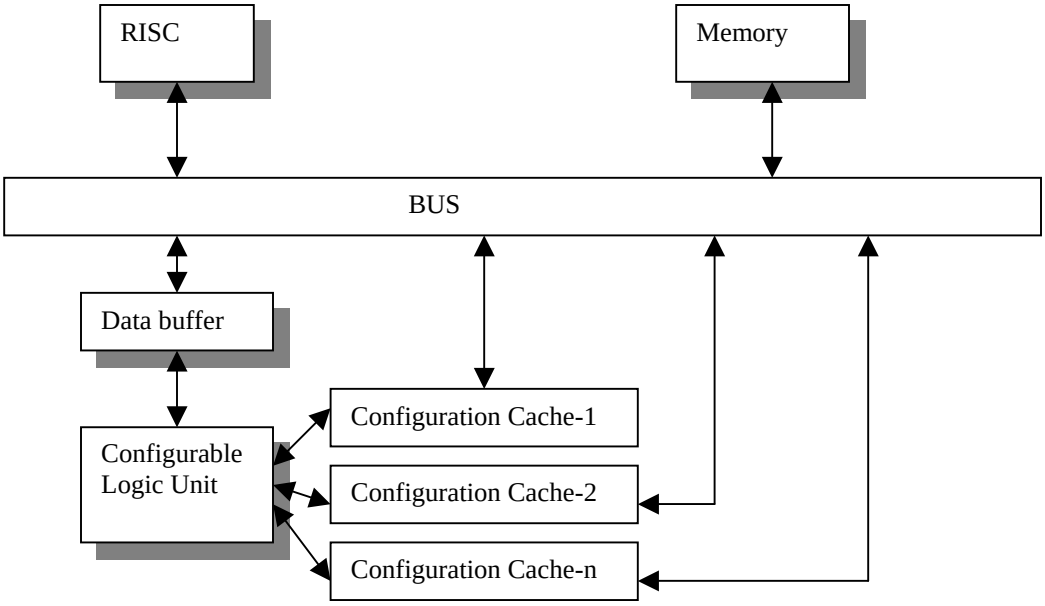
Finding MAX of A, B, C

1. Store A in (1,1)
2. Store B in (1,2)
3. Store C in (1,3)
4. (1,1) broadcasts its value to (1,2) and (1,3) thru horizontal bus 1
5. Other processors compare 2 values, its own value and the value received.

Mesh with bus is expensive due to buses. So reconfigurable mesh could be used to reduce bus utilization and power consumption

This falls under reconfigurable interconnection network.

Another way to improve existing architecture: Hybrid architecture



Hybrid System Architecture

Add-on card is inserted on the Memory bus and this add on card will be the reconfigurable block in the system

Reconfigurable hardware:

Advantages:
-Mentioned above-

Disadvantages:
This area is still in the state of infancy
FPGA technology needs improvement
Configuration time to be reduced
Not suitable for Floating point operations
Not suitable for fine grain structures because of lot of interconnections involved

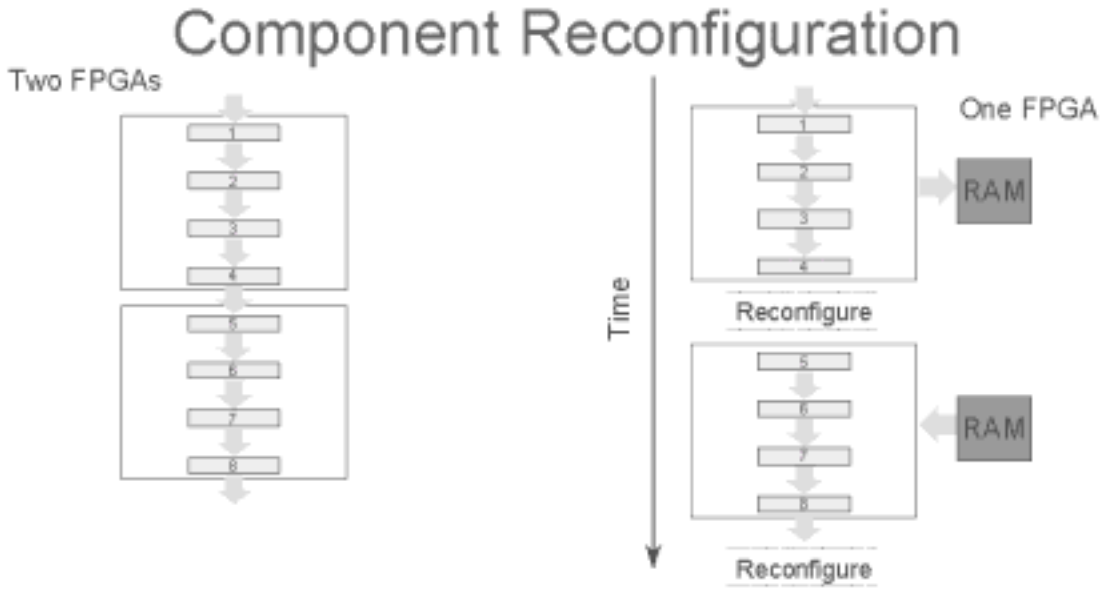
Recent trends and papers:

- Hardware accelerator for image processing

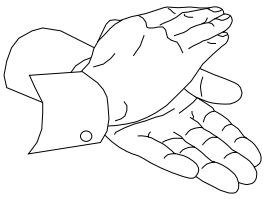
1. A vector coprocessor is also implemented either in a large FPGA or in an ASIC, allowing to speed-up applications where operations are performed on.
2. The system should be able to do digital signal processing in conjunction with graphics at real-time or near-real-time rates.
3. Where algorithmic complexity is too high for real-time computation, the system should be able to run asynchronously, storing the results for later display at synchronized real-time rates.

- Piperench – coprocessor for multi media acceleration

1. Uses Pipeline reconfiguration
2. Used where the application may require more hardware than what is available
3. Behaves like Pipelined hardware with different static configuration and each is loaded one per cycle into the hardware
4. Example: 2 stage is simulated in 1 stage device



Questions ?



END OF PRESENTATION