

Energy Savings in different coding schemes considering effects of both Substrate and Inter-wire Capacitances

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ABSTRACT

The power dissipation associated with driving data buses depends on both Substrate and Inter-wire capacitances. Lot of bus encoding schemes have been proposed to reduce the power dissipation in these buses. Most of the works focussed on minimizing the transitions. A previous work also considered the Inter-wire capacitance and proposed a coding scheme to reduce power dissipation. In this work I have considered both the Substrate, Inter-wire capacitances and calculated energy savings associated with each of the popular bus coding techniques. For this purpose run-time memory traces from Mediabench benchmark set have been extracted and used.

INTRODUCTION

Modern day digital processors use high capacitance buses to transmit data and hence lot of power has been dissipated for this. Several techniques have been proposed to reduce the power dissipation through the use of coding techniques which aim at reducing the number of transitions. But it has been shown [1] that transition reduction need not necessarily be the best approach for reducing power when effects of Interwire capacitances are considered. In this paper, energy consumed by databus has been simulated using bus data from a number of realistic benchmarks in conjunction with multiple encoding techniques. For this calculation the model proposed in [1] has been considered and this assumes that the distributive nature of the data lines is non-negligible for in sub-micron technologies lines are placed geometrically close to each other. So the interwire capacitances has to be considered with respect to substrate capacitances for actual power calculations.

BUS CODING TECHNIQUES

A number of bus coding schemes exist that code the value sent in the bus to be coded in the form that consumes less energy than the traditional twos complement representation. These schemes consider the only the effects of Substrate capacitance. So some coding schemes have been proposed that concentrates also on reducing energy lost due to Interwire capacitances. A paper[2] also discusses an adaptive bus coding scheme that will reduce the transition activity by exploiting value repetition. It has been shown in the work that this scheme is proved to be effective and produce better results than most of the coding techniques. Even this work focusses on reducing number of transitions hence it does not consider the effects of Interwire capacitances. This present work is to compare the efficiency of all these coding schemes considering a simple model of the databus and not ignoring the effects of relative transitions between bus lines. The schemes under consideration are as follows (refer [5] for details):

- Two's complement
- Gray code
- Signed Magnitude
- Bus Invert coding
- Adaptive bus coding

BENCHMARKS

Mediabench multimedia benchmark set[3] has been used to extract run-time bus activity since this is very representative of mobile applications. The actual data used is the subset of this benchmark. The traces were collected by porting Mediabench to the simple scalar architecture[4] and using the modified version of simple scalar simulator to dump memory access data traces. The width of the data bus is considered to be 32. A list of the benchmarks follows (refer [3] for details):

- Epic: Experimental Image Compression
- G721: CCITT based voice compression
- Jpeg: Lossy Image Compression
- GSM: European standard for speech transcoding

RESULTS

To evaluate the energy savings in each of the coding schemes software[8] was developed to calculate energy consumed during data transmission in various coding schemes for these benchmarks. In this calculation energy overhead of coding and decoding logic is not considered. Figures 1, 2, 3 and 4 show the energy consumption in data buses for these benchmarks for different capacitance ratios. This ratio plays an important part of energy consumption associated with the interaction of adjacent lines and this value is the ratio of Interwire to Substrate capacitance which is purely based on the technology parameters. Energy savings for each coding schemes relative to the standard twos complement coding are calculated and the results for Capacitance ratio = 0 (ignoring Interwire capacitance) are compared with the similar results produced in one of the previous works[6] and the results concur with each other. To check Adaptive coding technique, a synthetic benchmark[7] has been used and the energy savings are compared with the manual calculation.

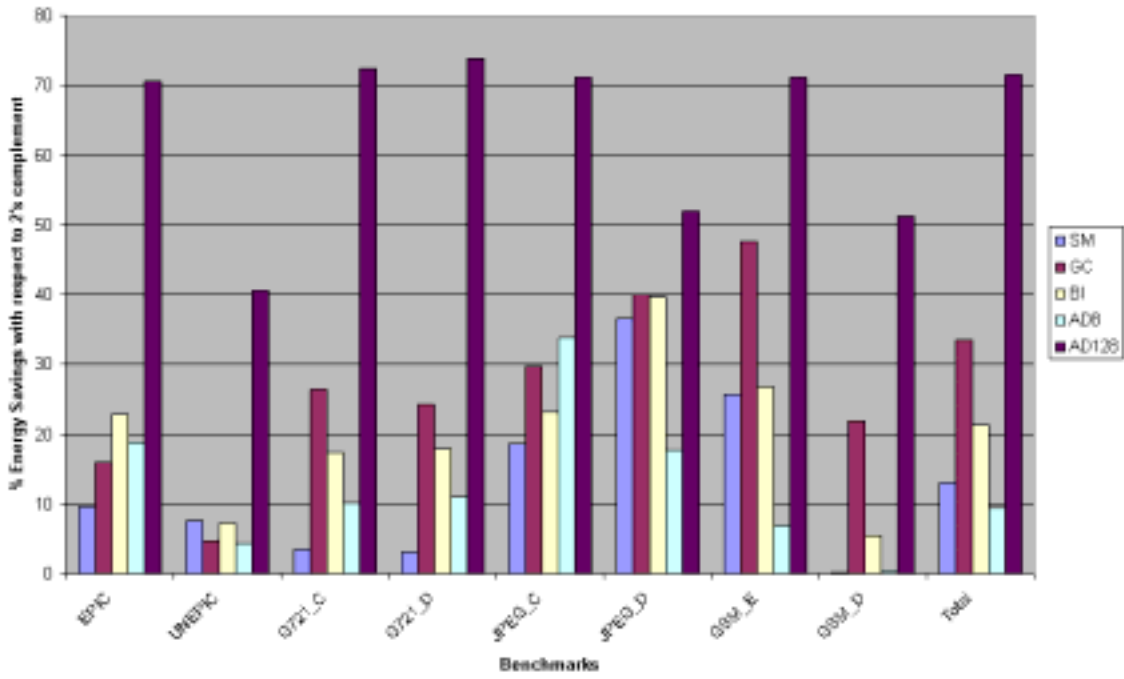
CONCLUSION

In this work some of the low power coding techniques have been considered and percentage energy savings of these schemes with respect to twos complement coding are calculated. It is based on an model for the data bus that explicitly considers the inter-wire capacitance. It was observed that percentage energy savings for these coding techniques decrease as the capacitance ratio increases. The coding schemes should be modified to incorporate effect of Interwire capacitance also to reduce overall power consumption so that decrease in energy savings due to increase in capacitance ratio is less. Adaptive technique shows better energy savings than all other coding techniques. Even for a LUT of size 8 it gives good energy savings comparing with traditional approaches. For a LUT of size 128 the increase in energy savings in all the benchmarks is very high. It can be concluded that either the coding scheme in [1] or the Adaptive coding scheme in [2] can be used to decrease energy consumption where inter-wire capacitance is non-negligible comparing to Substrate capacitance.

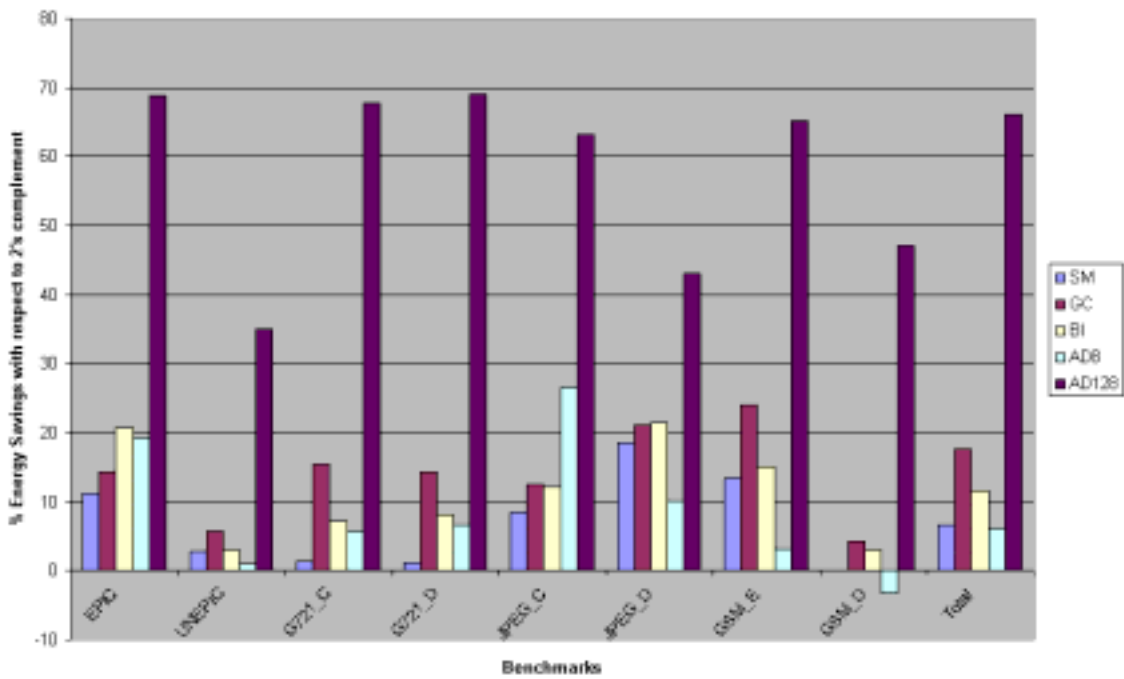
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- [7] <http://www.arches.uga.edu/~kaarthik/busCoding/test>
- [8] <http://www.arches.uga.edu/~kaarthik/busCoding/energy.tar.gz>

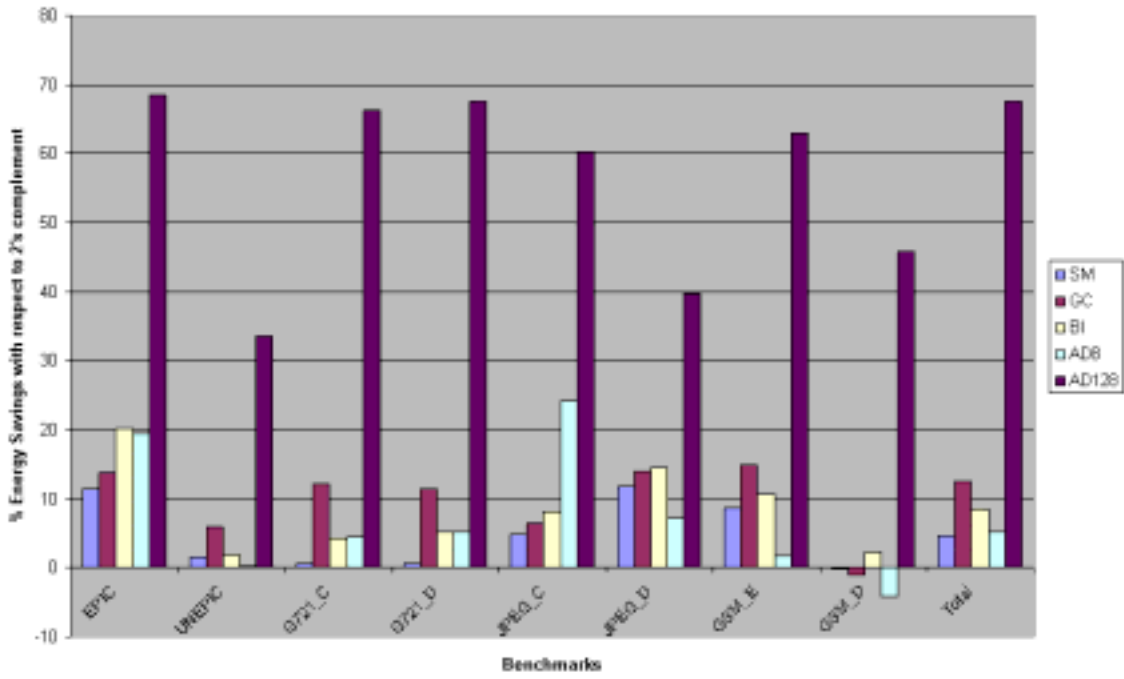
Energy Savings for Capacitance Ratio = 0



Energy Saving for Capacitance Ratio = 1



Energy Savings for Capacitance Ratio = 2



Energy Savings for Capacitance Ratio = infinity

